In the claims:

1. (Original) A method of receiving and outputting a plurality m of queues of data traffic streams to be switched from data traffic line card input ports to output ports, that comprises, providing a plurality n of similar successive data memory channels each having a number of memory cells defining a shared memory space assigned to the m queues; providing buffering for m memory cells in front of each memory channel to receive and buffer data switched thereto from line card traffic streams, and providing sufficient buffering to absorb a burst from up to n line cards; and distributing successive data in each of the queues during fixed limited times only to corresponding successive cells of each of the successive memory channels and in striped fashion across the memory space, thereby providing non-blocking shared memory output-buffered data switching.

2. (Original) The method of claim 1 wherein, in read mode, each line card draws data from storage in the shared memory through a corresponding buffer and in a fixed limited time slot to read out the required amount of data to satisfy its bandwidth needs.

3. (Original) The method of claim 1 wherein the buffering is provided by FIFO buffers each sized to store m cells of data.

4. (Original) The method of claim 3 wherein the aggregation of bandwidth to memory is adjusted for matching the data input bandwidth.

5. (Original) The method of claim 4 wherein the cell addresses are assigned continually such that the memory channels absorb said burst.

6. (Original) The method of claim 5 wherein in the event that all traffic streams from the line card ports are directed to one queue, accumulation of data is prevented in any FIFO by said matching.

7. (Original) The method of claim 5 wherein, in the event that all cells storing different queues happen to end on the same memory channel, the occurrence of a burst is absorbed on the FIFO at the front end of that channel.

8. (Original) The method of claim 7 wherein a subsequent burst is directed to the next successive memory channel of the memory space.

9. (Original) The method of claim 3 wherein the depth of each FIFO is adjusted to about the number m of queues.

10. (Original) The method of claim 2 wherein each buffer is a FIFO buffer sized for m cells of data.

11. (Original) The method of claim 3 wherein the number of input and output ports is scalable.

12. (Original) The method of claim 3 wherein 256 megabytes x n memory channels are employed.

13. (Withdrawn) A scalable-port, non-blocking, shared-memory output-buffered variable-length queued data switch.

14. (Currently amended) ~~An output - buffered switch as claimed in claim 13~~ A scalable-port, non-blocking, shared-memory output-buffered variable-length queued data switch wherein a data write path is provided having, in combination, a plurality of data line card input ports connected to a switch for switching m queues of data to a shared memory space assigned to the queues and comprising a plurality n of similar successive data memory channels, each having memory cells; a plurality n of buffers each fed data by the switch and each gated to feed a corresponding memory channel but only for fixed limited times; each of the buffers being provided with sufficient buffering to absorb a burst from up to n line cards; and means for distributing the successively gated data in each of the queues to corresponding successive cells of each of the

successive memory channels in striped fashion across the memory space, thereby to provide non-blocking, shared-memory output-buffered data switching.

15. (Original) The shared memory output-buffered switch of claim 14 wherein a read path is provided for each line card to draw data from storage in the shared memory through a corresponding buffer and in a fixed limited time slot to read out the required amount of data to satisfy its bandwidth needs.

16. (Original) The output-buffered switch of claim 14 wherein the buffering is provided by FIFO buffers each sized to store m cells of data.

17. (Original) The output-buffered switch of claim 16 wherein the aggregation of bandwidth to memory is adjusted for matching the data input bandwidth.

18. (Original) The output-buffered switch of claim 17 wherein means is provided for continually assigning the cell addresses such that the memory channels absorb said burst.

19. (Original) The output-buffered switch of claim 18 wherein, in the event that all traffic streams from the line card ports are directed to one queue, means is provided for preventing accumulation of data in any FIFO.

20. (Original) The output-buffered switch of claim 18 wherein, in the event that all cells storing different queues happen to end on the same memory channel, the occurrence of a burst is absorbed on the FIFO at the front end of that channel.

21. (Original) The output-buffered switch of claim 20 wherein means is provided for directing a subsequent burst to the next successive memory channel.

22. (Original) The output-buffered switch of claim 16 wherein the depth of each FIFO is adjusted to about the number m of queues.

23. (Original) The shared memory output-buffered switch system of claim 15 wherein each buffer is a FIFO buffer sized for m cells of data.

24. (Original) The shared memory output-buffered switch system of claim 23 wherein the line card drawing from shared memory is effected in a TDM type fashion.

25. (Withdrawn) A scalable-port, non-blocking, shared-memory output-buffered variable-length queued data switch connected to support 64 OC-192 or 16 0C-768 ports.

26. (Original) The method of claim 2 wherein the line card drawing from shared memory is effected in a TDM type fashion.